forming a cap on said second layer of sacrificial material, said cap forming a sealed cavity containing said microstructure and said first and said second sacrificial layers;
forming one or more holes in said sealed cavity, said holes being restricted to an area of said sealed cavity not directly above said microstructure;
introducing oxygen plasma into said sealed cavity through said one or more holes using a barrel etcher, said structural material and said sacrificial material having a high etch rate differential with respect to said oxygen plasma, such that said sacrificial material is removed; and
sealing said one or more holes in said sealed cavity.

REMARKS

The Examiner has objected to amended Claim 1, line 7, for containing a period, thereby making the claim more than one sentence. In response, the Applicant has modified Claim 1 to remove the period from line 7 and has replaced it with a semicolon to put the claim in proper form.

The Examiner has rejected Claims 1-3, 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Muller, et al., Seefeldt, et al. and Mitchell, et al. The Examiner states that Muller teaches the steps of the claimed invention, except that Muller does not teach whether or not the etchant is liquid or non liquid. Muller teaches the use of hydrofluoric acid, a liquid which is introduced into the sealed cavity through one or more holes to etch the sacrificial material. Likewise, Seefeldt discloses the use of hydrofluoric acid vapor, which is introduced through holes for the same purpose. In response, the Applicant has modified Claim 1 to specify that the etchant be limited to oxygen plasma. This distinguishes the invention as claimed from both Muller and Seefeldt in this respect.

The Examiner also states that Mitchell specifies the use of a barrel reactor for introduction of a fluorine-containing etchant. However, no combination of Mitchell, Muller and Seefeldt discloses the use of an oxygen plasma etchant with a barrel etcher. The Applicant believes that the use of the barrel etcher renders the invention patentably distinct from the three cited references because of the time needed to successfully etch large portions of sacrificial material using the oxygen plasma through the holes in the cap.

The Examiner has rejected Claims 1-3, 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Muller in view of Yao. The Applicant met with the Examiner on

July 8, 2002 to discuss the patentability of the invention and wishes to thank the Examiner for his time. It was agreed during this meeting that the introduction of evidence showing that the use of a dry etchant, specifically oxygen plasma, to etch the sacrificial material and release an encapsulated MEMS device was not conventional wisdom at the time of the invention would overcome the rejections wherein Yao is concerned. The Applicant submits that the use of a plasma etching agent for this purpose was not conventional wisdom at the time of the invention because the etch rates in a confined area, such as in an encapsulated cavity, are extremely low when a non-liquid etchant is used, resulting in the very long etch times. The low etch rates are the result of the small aspect ratio vias which must be used when releasing encapsulated MEMS devices, which require the etching of a relatively large area through very small openings. The difficulty arises because of the problem of removing etch by-products from the etch passage and introducing fresh etchant into the areas to be etched.

In support of this position, the Applicant has attached hereto the following evidence. In Appendix A, the Applicant has attached an article entitled *Selective, Deep Si Trench Etching with Dimensional Control,* Shul, et al, SPIE Conference on Micromachining and Microfabrication Process Technology IV (1998). A section of this reference beginning on page 257 and labeled "3.3 Aspect ratio dependent etching (ARDE)" shows that the smaller the aspect ratio, the more difficult it is to etch tunnels in a sacrificial material of any great length. The article states: "The difference [in the two examples shown] in etch depth is attributed to transport of reactants and etch products into and out of the trenches. As lateral dimensions decrease or the etch depths increase, it becomes more difficult for the reactive etch species to reach the bottom of the trench and more difficult for etch products to be removed." Thus, the problem of etching long distances utilizing small entry holes was well recognized as of the writing of this article in 1998, and conventional wisdom at the time was to use liquid etchants to etch encapsulated devices, especially if the etching of the device was to be commercially feasible. Also, it can be seen from Figure 8 that etch rate drops off precipitously for smaller via diameters. The graph shows etch via diameters from 0-3000 μM. The Applicant is etching large areas through holes as small as .5 μM in diameter. Thus, this reference teaches away from the use of a plasma etchant and supports the Applicant's position that conventional wisdom at the time of the invention was away from plasma etchants in favor of liquid etchants.

A similar result is provided by the article in Appendix B, attached hereto, entitled *Advanced Silicon Trench Etching in MEMS Applications*, Kühl, et al., SPIE Conference

on Micromachining and Microfabrication Process Technology IV(1998). Section 2.4 of this reference, entitled "2.4 Interdependence between etch rate and geometrical openings," starting on page 99, discusses the interdependence between etch rate and the size of via openings, showing that the smaller the aspect ratio of the tunnel being etched, the longer the etch time. The graph shown in Figure 4 shows etchings between approximately 1 and 12 μM in diameter, with etch rates dropping off precipitously with via diameters of around 1 μM. As previously stated, the Applicant is etching through holes approximately .5 μM in diameter. Holes of this size were not even considered in the studies because of the extremely low etch rates.

Also attached hereto in Appendix C, is the Affidavit of Dr. L. Richard Carley. Dr. Carley is a recognized expert in the field of MEMS, having a doctorate in Electrical Engineering and Computer Science from M.I.T. and having worked in the MEMS field for at least eight years in his capacity as a Professor in the Electrical Engineering Department of Carnegie Mellon University, Pittsburgh, and as Chief Executive Officer and Chief Technology Officer of IC Mechanics, Inc. of 425 North Craig Street, Pittsburgh, PA, a company specializing in the commercial development of MEMS devices. Dr. Carley currently holds two MEMS-related patents, has authored or co-authored and published at least 24 papers in the MEMS area and has been the Principal Investigator or co-Principal Investigator on five major federally sponsored MEMS research programs. Dr. Carley states that, to his knowledge as en expert in the MEMS field, at the time of this invention, he was unaware of anyone using plasma as an etchant for releasing encapsulated MEMS devices, principally because of the extremely long etch period required when using small aspect ratio vias to introduce the etchant and to etch large areas under the cap.

The Applicant has also, in the last office action, made similar articles part of the record in the application. In particular, the Applicant refers the Examiner to Exhibit A filed with the Preliminary Amendment, dated April 30, 2002, which quotes a passage a book entitled *Fundamentals of Microfabrication*, which states that "only wet etchings can be used" and that, "undercutting wide areas with BHF can take hours" to remove the sacrificial spacer in an encapsulated MEMS device. This passage is probably the most important in terms of defining the conventional wisdom regarding removal of sacrificial layers at the time of the invention.

CONCLUSION

The Applicant has modified Claim 1 by adding the limitation that the non-liquid etchant used be oxygen plasma, thereby traversing the Examiner's rejection of the claims under 35 U.S.C. § 103(a) based on the combination of Muller, et al., Seefeldt, et al and Mitchell, et al. Additionally, the Applicant has provided anecdotal evidence of the conventional wisdom regarding the removal of sacrificial material to release an encapsulated MEMS device in the form of articles and an Affidavit from a recognized expert in the field, to overcome the Examiner's rejection under 35 U.S.C. § 103(a) based on the combination of Muller and Yao.

Accordingly, the Applicant respectfully submits that the application as amended is in condition for immediate allowance and requests that the Examiner allow the Application at the earliest possible time, based on the amendments and remarks herein.

Respectfully submitted,

Dennis M. Carleton
Reg. No. 40,938
Buchanan Ingersoll, P.C.
One Oxford Centre, 20th Floor
Pittsburgh, PA 15219
(412) 562-1895
e-mail: carletondm@bipc.com

Attorney for Applicant

#1194307

ADDENDUM
(Marked Up Claims)

1. (Amended) A method of fabricating a microstructure in a sealed cavity comprising the steps of :

providing a substrate;

forming a microstructure composed of a structural material on said substrate, said microstructure being secured to said substrate by a first layer of sacrificial material;

forming a second layer of sacrificial material on said microstructure;

forming a cap on said second layer of sacrificial material, said cap forming a sealed cavity containing said microstructure and said first and said second sacrificial layers[.];

forming one or more holes in said sealed cavity, said holes being restricted to an area of said sealed cavity not directly above said microstructure;

introducing [a non-liquid etchant] oxygen plasma into said sealed cavity through said one or more holes using a barrel etcher, said structural material and said sacrificial material having a high etch rate differential with respect to said [etchant] oxygen plasma, such that said sacrificial material is removed; and

sealing said one or more holes in said sealed cavity.

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SELECTIVE, DEEP Si TRENCH ETCHING WITH DIMENSIONAL CONTROL

R. J. Shul, C. G. Willison, and L. Zhang

Sandia National Laboratories, Albuquerque, New Mexico 87185-0603

ABSTRACT

The recent development of a high-aspect ratio Si etch (HARSE) process[1] has enabled the fabrication of a variety of Si structures where deep trench etching is necessary. The HARSE process relies on the formation of a sidewall etch inhibitor to prevent lateral etching of the Si structures during exposure to an aggressive SF_6/Ar plasma etch chemistry. The process yields highly anisotropic profiles with excellent dimensional control for high aspect ratio features. In this study, Si etch rates and etch selectivities to photoresist are reported as a function of chamber pressure, cathode rf-power, ICP source power, and gas flow. Si etch rates > 3 μm/min with etch selectivities to resist > 75:1 were obtained. Lateral dimensional control, etch selectivities to SiO_2 and Si_3N_4, and aspect ratio dependent etching (ARDE) will also be discussed.

Keywords: high-aspect ratio silicon etching, inductively coupled plasma etching, aspect ratio dependent etching, dimensional control.

1. INTRODUCTION

Pattern transfer into Si has been very successful by both wet chemical and plasma etch techniques.[2-6] However, the fabrication of deep, high-aspect ratio Si structures has been limited due to low etch selectivity to photoresist masks, slow etch rates, or poor lateral dimensional control. For example, wet chemical etching is typically fast, often exceeding several μm/min, but can be isotropic, crystallographic, and difficult to control. Reactive ion etching (RIE) of Si in either chlorine or fluorine based plasmas can yield anisotropic, non-crystallographic, highly directional etching but at rates typically < 0.5 μm/min. High-density plasma (HDP) etching including electron cyclotron resonance (ECR) etching and inductively coupled plasma (ICP) etching can result in rates > 2.5 μm/min with anisotropic profiles (at temperatures < 0°C) but aspect ratios that are typically ≤ 10:1. Another disadvantage of RIE and HDP deep etching of Si is the low selectivity to photoresist (and thus the need for hard masks) due to the high ion energies necessary to achieve high etch rates and anisotropic profiles. The recent development of a high-aspect ratio Si etch (HARSE) process has resulted in anisotropic profiles at room temperature, etch rates > 3.0 μm/min, aspect ratios > 30:1, and good dimensional control.[1] Additionally, the HARSE process has shown etch selectivities of Si to photoresist > 75:1 thereby eliminating the process complexity of hard etch masks for features deeper than 100 μm.

The HARSE process (patented by Robert Bosch GmbH)[1] relies on an iterative ICP-based deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during the deposition cycle. The polymer deposits over the resist mask, the exposed Si field, and along the sidewall. During the ensuing etch cycle, the polymer film is preferentially sputtered from the Si trenches and the top of the resist mask due to the acceleration of ions (formed in the ICP plasma) perpendicular to the surface of the wafer. Provided the ion scattering is relatively low, the polymer film on the sidewall is removed at a much slower rate, thus minimizing lateral etching of the Si. Before the sidewall polymer is completely removed, the deposition step is repeated and the cycle continues until the desired etch depth is obtained. In this study we report Si etch results using the HARSE process as a function of pressure, cathode rf-power, ICP source power, and gas flow. These results are compared to Si etch results obtained in a SF_6/O_2-based ICP plasma.

2. EXPERIMENTAL

Si wafers were patterned with AZ-4330 photoresist, which was spun on to a thickness of approximately 3.4 μm. The Si etch results were obtained in a load-locked Plasma-Therm SLR 770 ICP etch system with a Plasma-Therm 2 MHz ICP source. Energetic ion bombardment was provided by superimposing an rf-bias (13.56 MHz) on the sample. Samples were mounted with a low vapor pressure thermal paste onto a 6 inch Si wafer carrier that was coated with approximately 1 μm of thermal SiO_2 to minimize loading effects. The Si wafer carrier was clamped to the cathode and cooled to 20°C with He gas. Process

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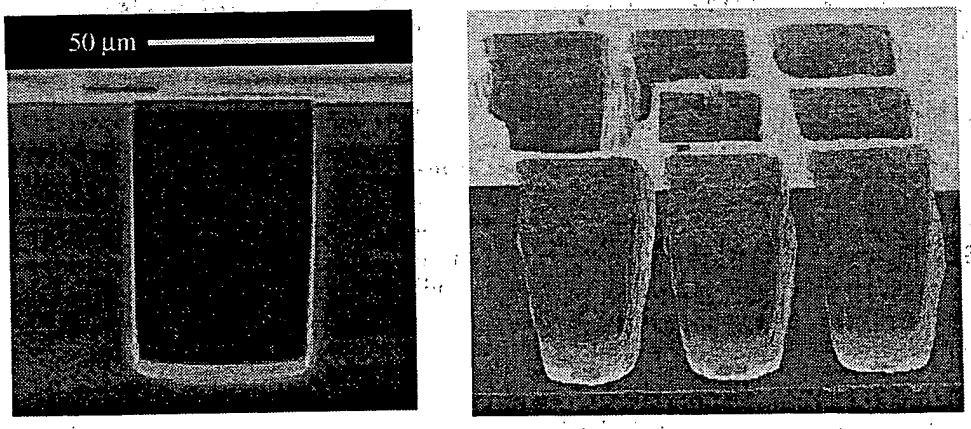
gases were introduced through an annular region at the top of the chamber. Si etch rates were calculated from the depth of the etched feature measured with an Alpha Step stylus profilometer following removal of the photoresist. Samples were exposed to the plasma for 10 minutes and all depth measurements were taken on 20 μm wide features in a minimum of three positions. Each sample was approximately 1 cm^2. Selectivities were reported as the ratio of Si etch rate to resist erosion rate. The resist erosion rate was calculated from the depth of the resist measured with the profilometer before and after exposure to the plasma relative to the depth of the Si removed during the etch. Etch profile and morphology were evaluated using a scanning electron microscope (SEM).

3. HARSE RESULTS

3.1 HARSE versus ICP etch comparison

As stated earlier, Si can be etched in an ICP SF_6-based plasma at relatively high rates, however good dimensional control and smooth etch morphology can be difficult to achieve. In Figure 1, SEM micrographs show Si vias etched by (a) the HARSE process and (b) an ICP-generated SF_6/O_2 plasma. The via etched using the HARSE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm. The HARSE etch conditions were 23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 875 W ICP source power, 6 W cathode rf-power with a corresponding dc-bias of –25 to –50 V, and 20°C substrate temperature. The ICP etch conditions were 5 mTorr pressure, 50 sccm SF_6, 10 sccm O_2, 10 sccm Ar, 500 W ICP source power, 250 W cathode rf-power with a corresponding dc-bias of -350 V, and -40°C substrate temperature. Due to the high dc-bias used in the ICP, the etch selectivity of Si to photoresist was typically ≤ 2:1; therefore, a Ni mask was used to achieve etch depths > 25 μm. The ICP etch rate was approximately 1 μm/min. The HARSE process used a photoresist mask due to etch selectivities > 75:1. The high etch selectivity observed in the HARSE process is attributed to the deposition of the sidewall polymer etch inhibitor, which also deposits on the resist. Despite ion bombardment of the surface, the deposited polymer significantly reduces the erosion rate of the resist. Additionally, lower dc-biases in the HARSE process (≤ -50 V as compared to -350 V in the ICP) significantly reduce the resist erosion rate. The HARSE process yielded an etch rate of approximately 2.0 μm/min with highly anisotropic etch profiles, good dimensional control, and smooth etch morphologies. The sidewall polymer etch inhibitor deposited in the HARSE process eliminated lateral etching of the Si resulting in via widths which were essentially identical at the top and bottom of the feature. However in the ICP, lateral etching of the Si was observed due to the absence of a sidewall polymer resulting in poorly controlled via profiles. The sidewall profile was concave with a much wider opening at the top of the via than that obtained at the bottom. Additionally, the sidewall was much rougher than that achieved using the HARSE process. The lateral Si etching observed in the ICP was somewhat surprising due to the low process pressure (2 mTorr) which reduces ion scattering and sidewall sputtering and the low substrate temperature (-40°C) which lowers the volatility of the etch products.



(a) (b)

Figure 1. SEM micrographs which show Si vias etched by (a) the HARSE process and (b) an ICP-generated SF_6/O_2 plasma. The via etched using the HARSE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm.

3.2 Etch rates and selectivity

In order to evaluate the HARSE process for device application, etch parameters were studied as a function of chamber pressure, cathode rf-power, ICP source power, and SF_6 flow rate. In Figure 2, Si etch rates and etch selectivity of Si to photoresist are shown as a function of pressure while the cathode rf-power, ICP source power, gas flows, and substrate temperature remained constant. Plasma conditions change quite dramatically as a function of pressure, in particular the mean free path decreases, the collisional frequency increases, and the residence time of the reactive species increases as the pressure is increased. This typically results in changes in both ion energy and plasma density which strongly influences the etch properties. Si etch rates increased as the pressure was increased from 15 to 20 mTorr, suggesting a reactant limited regime at low pressures. Above 20 mTorr, the Si etch rate was relatively independent of pressure. Selectivity of Si to photoresist was typically > 50:1 with a maximum of approximately 95:1 at 25 mTorr. Etch profile and morphology were relatively independent of pressure.

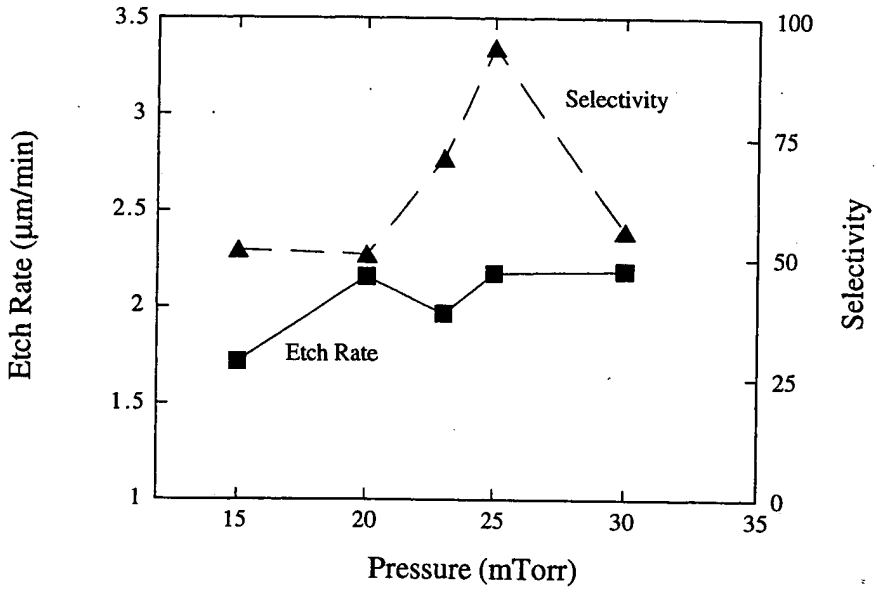


Figure 2. Si etch rates and etch selectivity of Si to photoresist as a function of pressure in the HARSE process.

Etch characteristics normally show a strong dependence on ion energy and plasma density. Ion energies influence the physical component of the etch whereas plasma density can affect both the physical and chemical components of the process. In Figure 3, Si etch rates and etch selectivity of Si to photoresist are plotted as a function of cathode rf-power while all other plasma parameters were held constant. Si etch rates increased monotonically by almost a factor of 3 as the cathode rf-power increased. Since cathode rf-power is closely related to dc-bias and ion bombardment energy, higher etch rates at higher ion energies implies more efficient bond breaking of the Si surface bonds and improved sputter desorption of the etch products (i.e. SiF_x) from the surface. As the ion bombardment energy increased so did the sputtering efficiency of the polymer in the Si field which was deposited during the deposition cycle of the HARSE process. Under low rf-power conditions, the polymer may not sputter as efficiently thereby increasing the etch initiation time and reducing the Si etch rates. Despite faster Si etch rates, the etch selectivity decreased quite dramatically as the cathode rf-power increased due to faster sputter rates of the polymer and faster erosion rates of the resist.

Dimensional control and etch profile were strongly dependent on cathode rf-power. Under low cathode rf-power conditions, the etch profile was positively tapered. At moderate cathode rf-powers, the profile was highly anisotropic. Finally, under high cathode rf-power conditions, the profile became re-entrant. This trend can be observed in Figures 4 and 5. In Figure 4, SEM micrographs show Si posts etched at (a) 8 and (b) 25 W cathode rf-power. At 8 W, the etch profile was highly anisotropic at an etch depth of approximately 23 μm. At 25 W, the etch depth was approximately 30 μm and a

prominent re-entrant profile was observed. The re-entrant profile observed under high rf-power conditions was attributed to more ion scattering at the base of the feature and higher sputter removal rates of the polymer from the Si sidewall.

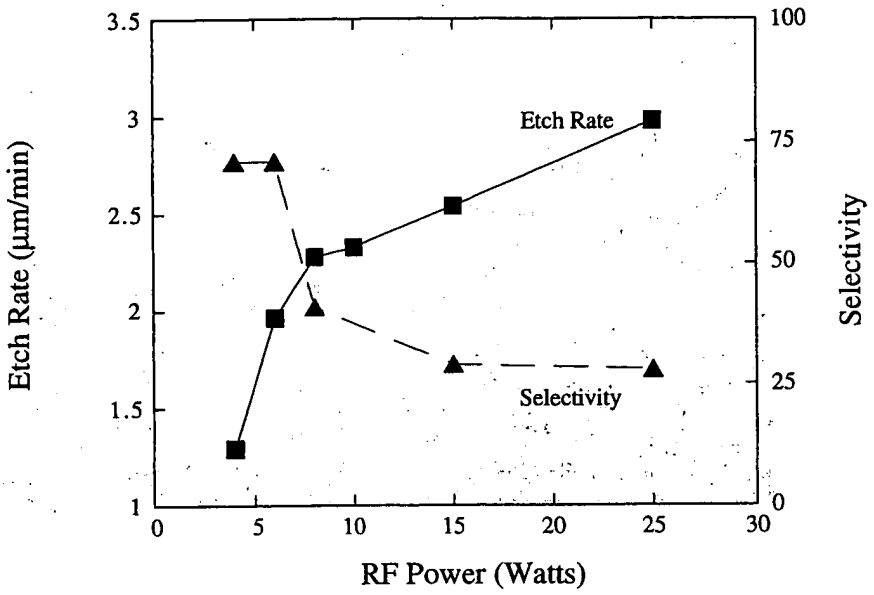


Figure 3. Si etch rates and etch selectivity of Si to photoresist as a function of cathode rf-power for the HARSE process.

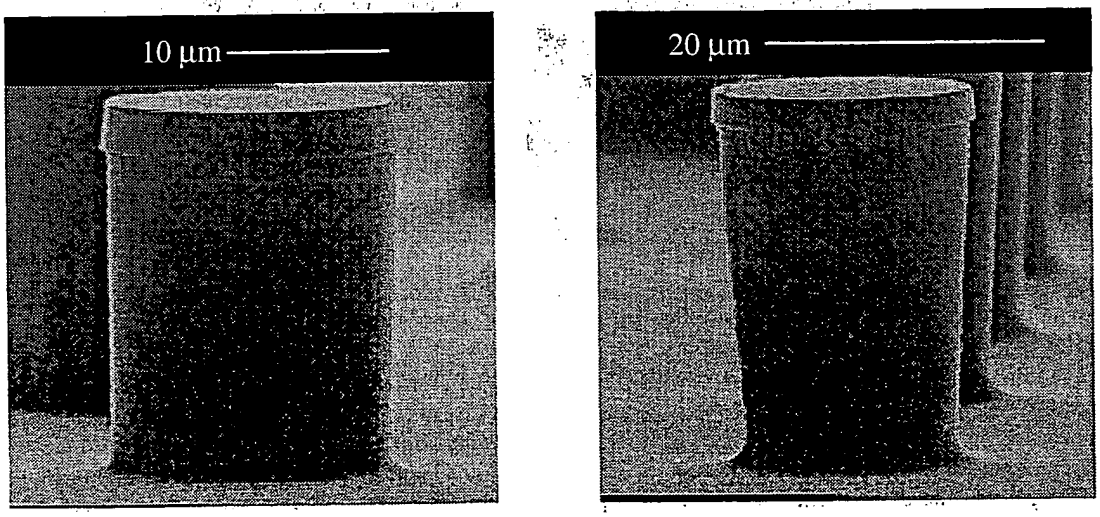


Figure 4. SEM micrograph of Si posts etched at (a) 8 W and (b) 25 W cathode rf-power. The re-entrant profile observed at 25 W cathode rf-power was attributed to increased ion scattering and sputter removal of the sidewall polymer.

In Figure 5, Si trenches 15 to 20 μm wide were etched approximately 70 μm deep. In Figure 5a, the HARSE process was run at 6 W cathode rf-power for 30 minutes. The etch rate was approximately 2 μm/min at a dc-bias of approximately -50 V. The trench profile showed a positive taper and significant roughness at the bottom while the sidewall at the top remained smooth. The rough etch morphology at the bottom of the trench was attributed to inefficient sputter

removal of the deposited polymer due to ineffective ion transport. In Figure 5b the standard etch was run for 20 minutes followed by a more aggressive etch (8W cathode rf-power and 22% longer etch cycle) for 5 minutes and then completed with the standard process for another 5 minutes. The etch was approximately 15 μm deeper than the single step etch with an etch rate of approximately 2.5 μm/min. The etch was highly anisotropic with a slight foot at the base of the sidewall and a smooth sidewall morphology throughout the feature. At higher rf-power, the increased ion bombardment energy improved the sputter removal of the deposited polymer from the bottom of the trench and allowed chemical etching at the base of the Si trench. Therefore it is critical to optimize the sputter removal rate of the polymer from the base of the feature.

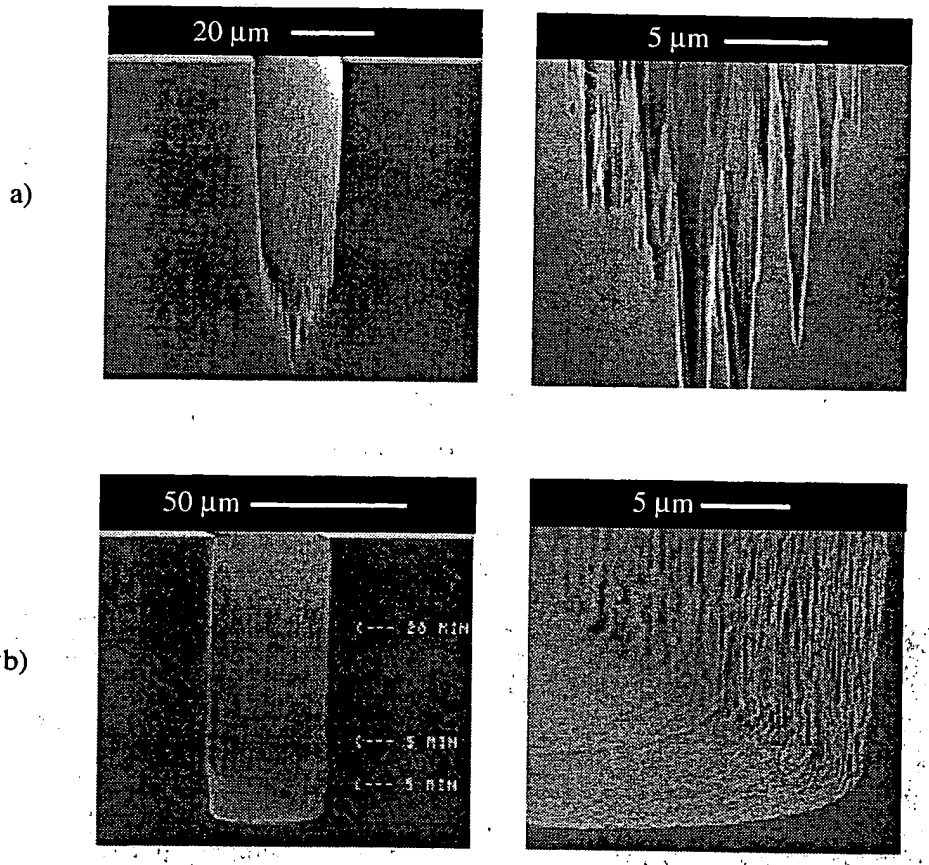


Figure 5. SEM micrograph of Si etched with a) single step HARSE process (6W cathode rf-power) and b) a three-step process with an aggressive step (8W cathode rf-power) to increase the sputter desorption at the base of the trench.

As a function of increasing plasma density or ICP source power, etch rates typically increase due to 1) higher concentrations of reactive species which increases the chemical component of the etch mechanism and 2) higher ion flux which increases the sputter desorption component of the etch mechanism. The effects of ion energies and plasma densities are more obvious for HDP systems, since ion energies and plasma densities can be more effectively decoupled as compared to RIE. In Figure 6, the Si etch rates increased by approximately 30% as the ICP source power increased. The etch selectivity data was less consistent ranging from approximately 55:1 to 90:1. The low selectivity observed at 800 W ICP source power is not understood. Etch profiles were slightly re-entrant and rough under low ICP source power conditions.

Si etch rates are also expected to increase with higher SF_6 flow rates due to the strong chemical component of the Si etch mechanism and higher concentrations of reactive F. In Figure 7, Si etch rates and selectivity to photoresist are plotted as a function of SF_6 flow rate. Si etch rates increased as the SF_6 flow rate increased from 60 to 120 sccm implying a reactant limited etch regime at low flow rates. However at 150 sccm SF_6 the etch rate decreased significantly indicating a diffusion limited regime. The etch selectivity was quite low (< 50:1) except at 80 sccm where the selectivity was >120:1. Etch profile and morphology were essentially independent of SF_6 flow rates.

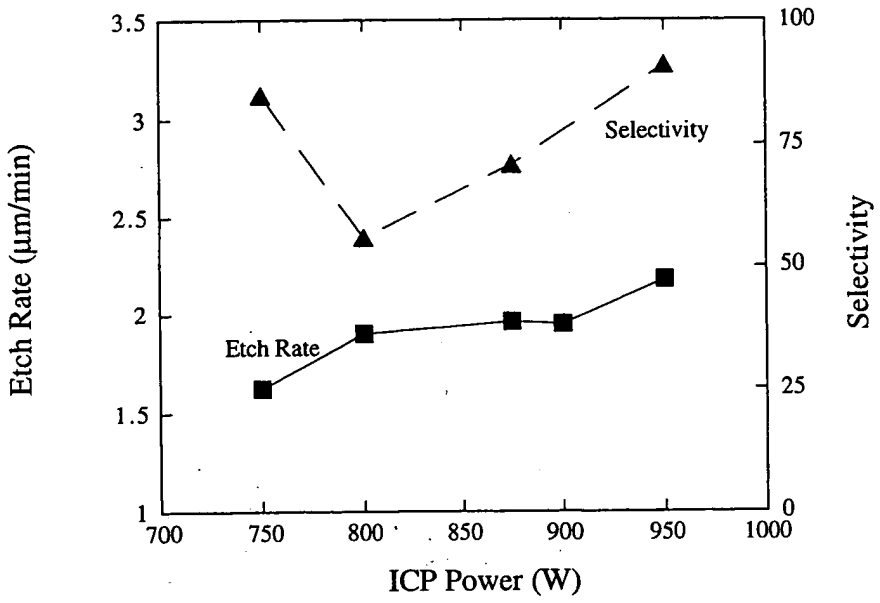


Figure 6. Si etch rates and etch selectivity of Si to photoresist as a function of ICP source power for the HARSE process.

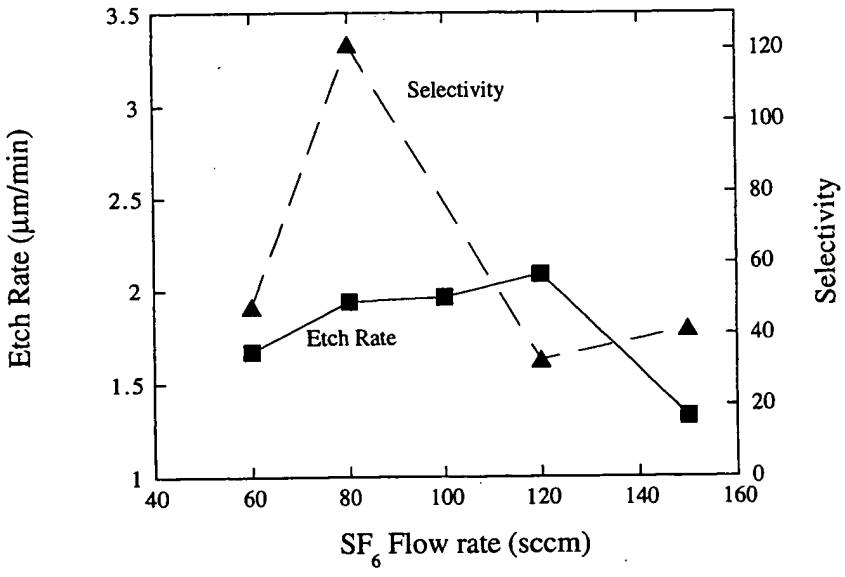


Figure 7. Si etch rates and etch selectivity of Si to photoresist as a function of SF_6 flow rate for the HARSE process.

3.3 Aspect rati dependent etching (ARDE)

The observation that smaller diameter vias and narrower trenches etch more slowly than larger diameter vias and wider trenches is often referred to as aspect ratio dependent etching (ARDE) or RIE lag.[7] An example of ARDE is shown in Figure

8 for 1 and 3.5 μm wide trenches. The etch depth for the 1 μm trenches was approximately 7.5 μm while the 3.5 μm trenches were etched to a depth of approximately 9.5 μm. The difference in etch depth is attributed to transport of reactants and etch products into and out of the trenches.[7] As lateral dimensions decrease or the etch depths increase it becomes more difficult for the reactive etch species to reach the bottom of the trench and more difficult for etch products to be removed. Ayon and coworkers have observed improved ARDE effects for the HARSE process under high SF_6 flows conditions.[8] They attributed this observation to a reduction in etch product species that contribute to redeposition.

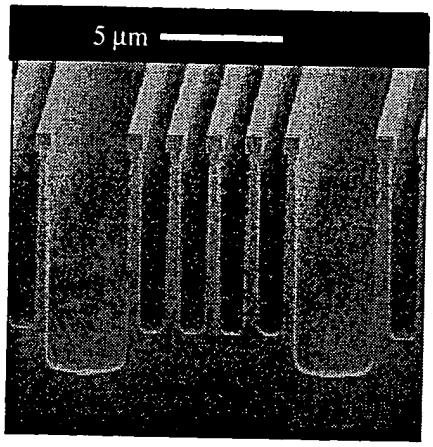


Figure 8. SEM micrograph of Si HARSE etch which demonstrates ARDE. The 1 μm wide trenches were etched to an approximate depth of 7.5 μm while the 3.5 μm trenches were etched to a depth of approximately 9.5 μm.

In Figure 9, Si etch depths are plotted as a function of via diameter for the HARSE process (23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 850 W ICP source power, 8W cathode rf-power, and 20°C substrate temperature) at 30, 60, and 90 minute plasma exposure times. As expected, the etch depths increased as a function of time. Also, as the via diameters increased from 10 to 300 μm, the etch depth typically increased independent of etch time. This was attributed to improved transport of reactants into the via and etch products out of the via as the diameter increased. Above 300 μm via diameter, the etch depth remained relatively constant independent of diameter for the 30 and 60 minute etches with only a slight increase for the 90 minute etch.

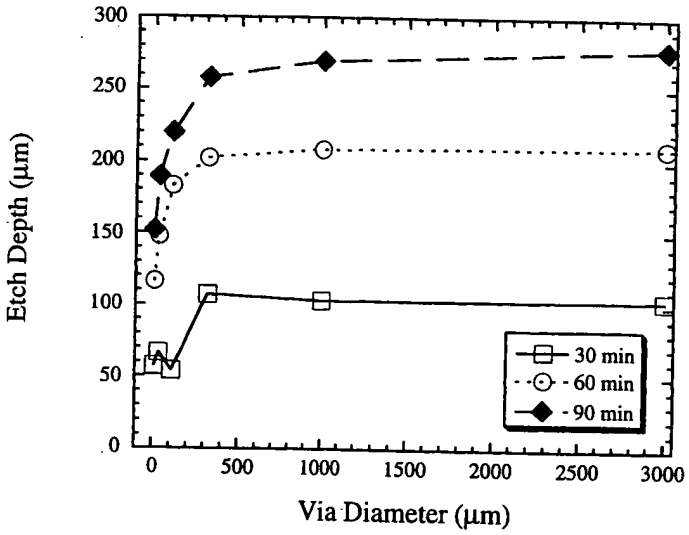


Figure 9. Si etch depths plotted as a function of via diameter for 30, 60, and 90 minute HARSE etch times.

3.4 Etch selectivities

Selective etching of one material over another is critical in the fabrication of microelectronic and photonic devices to accurately stop on defined layers for subsequent processing steps, for example the formation of ohmic and gate contacts. For high aspect-ratio silicon structures, selective etching is important in the fabrication of membrane-based devices where the etch process must stop on a thin film layer typically < 1 μm thick. Etch selectivities of Si to several films exposed to the HARSE process are shown in Table 1. HARSE etch conditions were 23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 850 W ICP source power, 8W cathode rf-power with a corresponding dc-bias of –25 to –50 V, and 20°C substrate temperature. As mentioned earlier, the high etch selectivity of Si to photoresist simplifies the process sequence for deep high-aspect ratio features by eliminating the need for hard masks. The high etch selectivities of Si to either SiO_2 or Si_3N_4, makes them excellent candidates for the membrane-based structures including flexural plate wave (FPW) devices and micromachined valves, pumps, and heaters.

Material	Etch Rate (Å/min)	Selectivity to Si
Si	25,000	
Polysilicon	5334	4.7:1
LPCVD Si_3N_4	295	85:1
LPCVD SiO_2	90	275:1
Thermal SiO_2	90	275:1
Photoresist	250	100:1

Table 1. HARSE etch rates and selectivity to Si.

A schematic diagram of a membrane-based device is shown in Figure 10. Initially, a thermal SiO_2 or low stress low pressure chemical vapor deposition (LPCVD) Si_3N_4 film is deposited on the frontside of the wafer. All frontside processing (metallization, etch, etc.) is completed and protected with photoresist. The Si via etch mask is then applied using a thick photoresist (AZ 4903) and aligned to the frontside membrane features using backside alignment techniques. The wafer is then exposed to the HARSE process (where 400 to 650 μm of Si is removed) and etched to the SiO_2 or Si_3N_4 membrane which is typically ≤ 1 μm thick. The results of this process sequence are demonstrated in Figure 11. The SEM micrograph shows a 400 μm wide Si via etched to a depth of approximately 685 μm at an etch rate of 3.5 μm/min. Due to the high etch selectivity of Si to SiO_2 (see Table 1), the etch essentially stops on the thermal SiO_2 layer which was 0.6 μm thick. The via was highly anisotropic and maintained the dimensions of the mask, however the sidewall morphology was somewhat rough due to vertical striations and a slight Si foot was observed at the base of the sidewall. Ayon and co-workers have also observed a foot at the base of many of their features.[8] Altering the deposition cycle of the HARSE process, they have been able to significantly reduce the foot dimesions. The features observed at the bottom of the via in Figure 11a were frontside metal features which could be seen through the transparent thermal SiO_2 film.

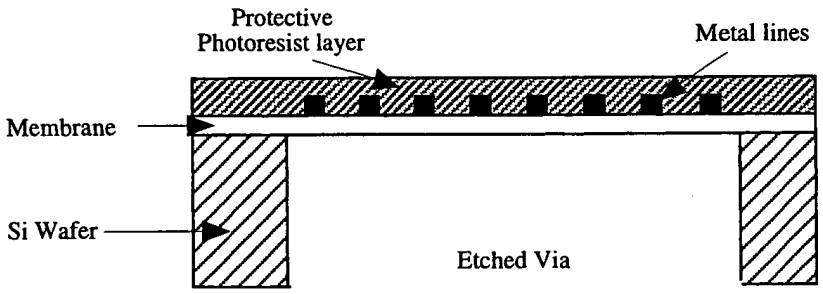
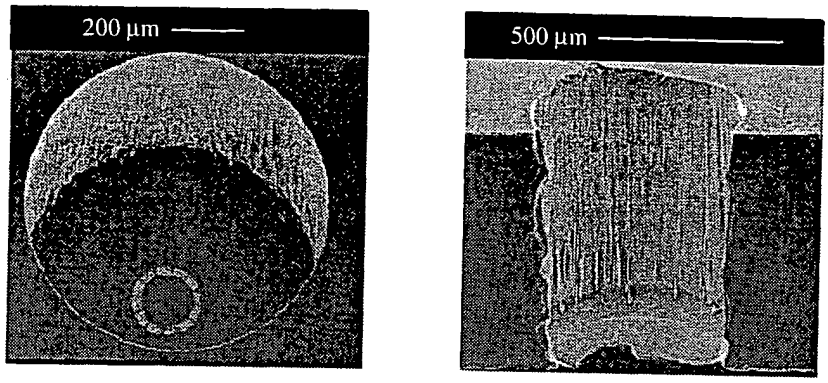


Figure 10. Schematic of a membrane based device with a HARSE via, a thin film membrane, frontside metal lines, and a protective photoresist layer.



(a) (b)

Figure 11. SEM micrographs of a Si via HARSE etched to a depth of approximately 685 µm to a thin thermal SiO_2 layer which acts as an etch stop. The via diameter was approximately 400 µm.

5. CONCLUSIONS

Etch rates ranging from 1 to 3.5 µm/min with highly anisotropic profiles and smooth etch morphologies were demonstrated for several HARSE process conditions. Si etch rates, profiles, dimensional control, and morphologies were strongly dependent on cathode rf-power. As the cathode rf-power or ion energy increased, the etch rate increased due to more efficient sputter removal of the polymer, more efficient bond breaking of the Si bonds, and more efficient sputter desorption of the etch products from the surface. Under low cathode rf-power conditions the etch profile was positively tapered due to inefficient sputter removal of the polymer; became highly anisotropic at moderate cathode rf-power; and was re-entrant under high cathode rf-power conditions due to ion scattering and sputter removal of the polymer from the Si sidewall. Si etch characteristics were much less dependent on chamber pressure, ICP source power, and SF_6 flow rate. The HARSE process operated at room temperature and showed etch selectivities of Si to resist > 75:1 thus eliminating the need for hard masks. Etch selectivities for Si to SiO_2 were 275:1 and to Si_3N_4 were 85:1 thus enabling the fabrication of membrane-based devices. ARDE was observed for small vias and trenches but was less significant for large features (≥ 300 µm).

6. ACKNOWLEDGMENTS

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Advanced silicon trench etching in MEMS applications

Karl Kühl[a], Stefan Vogel[a], Ulrich Schaber[a], Rainer Schafflik[b], Bernd Hillerich[a]

[a] Fraunhofer-Institut für Festkörpertechnologie, Hansastr. 27d D-80686 München, Germany
[b] Surface Technology Systems GmbH, Griesbadgasse 24 D-89073 Ulm, Germany

ABSTRACT

A high performance silicon dry etch process (STS Advanced Silicon Etch ASE) which in many cases is a beneficial replacement for the usual anisotropic wet etch methods like KOH etching is presented. During fabrication of Micro-Electro-Mechanical Systems (MEMS) the patterning of silicon is an essential step. Conventional wet or dry etching processes used up to now cannot meet the majority of future MEMS patterning needs. The process described in this paper allows a wide range of possible geometries and freedom of design and mask layout for novel MEMS applications. The installed etch system is working with an inductively coupled plasma source (ICP) which produces high plasma densities at low pressure to achieve deep silicon etching (> 200 µm) with high etch rates up to 5 µm/min and a high passivation layer selectivity. The new ASE process uses only fluorine based chemistry and operates at room temperature. ASE uses photoresists and silicon oxid layers as an etch passivation and allows the manufacturing of silicon structures with nearly vertical side walls in bulk and surface micromachining illustrated by several MEMS applications carried out at the Fraunhofer Institute for Solid State Technology. With depths up to 100 µm realized at the institute now and an excellent anisotropic profile control ASE is obviously the tool, useful from device development to volume production of microsystems.

Keywords: ASE process, deep Si etching, micromachining, microfabrication tool, MEMS application

1. INTRODUCTION

Wet chemistry using alkaline etchants depends upon the crystal orientation of the substrate and therefore on a fixed anisotropy and aspect ratio. This leads to a small freedom of design and in some cases to high consumption of chip space. Additionally it is necessary to use a bi-mask process prior to the wet etching. This causes a complex process flow and thus, high costs. The ever present compatibility problem with CMOS technology restricts the use of wet etch solutions. The dry etching of silicon using a standard capacitively coupled RIE plasma is only useful for shallow, low aspect ratio etching. There is however an increasing tendency to opt for high density low pressure (HDLP) systems like the one Surface Technology Systems Inc. has commercialized for the Advanced Silicon Etch (ASE) process developed by Robert Bosch GmbH [1] using an Inductive Coupled Plasma (ICP) system. A schematic of the STS ICP is shown in Figure 3.

2. THE ASE PROCESS TOOL

2.1 etch process steps

Due to the limits of the above mentioned techniques and to meet the goals for the majority of MEMS etch applications, STS has made an early investment in developing the ASE (Advanced Silicon Etch), which now provides a unique processing capability. This process is based on the technique invented by Lärmer and Schilp[1] and uses a variant of the sidewall passivation technique. In this case the passivation is deliberately segregated by using sequentially alternating etching and deposition steps.

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First a sidewall passivation polymer is deposited and subsequently the polymer and silicon are etched from the base of the trench, to allow the etching to proceed directionally. In this cyclic way the etching and deposition can be balanced to provide accurate control of the anisotropy.

During the deposition step, the precursor gas is dissociated at first by the plasma to form ion and radical species. A passivating layer is deposited on the surface of the silicon as well as on the mask. Figure 1 shows this first step of the ASE process schematically. The passivation layer is only built by the nCF_2 film, in contrast to other side wall passivation techniques generating reacted films like SiO_2.
The second step of the ASE process is the etch cycle. The gases are switched to allow etching. During this subsequent etch step, the SF_6 dissociates. Then the fluorine radicals have to remove the surface passivation layer, before the silicon etching can proceed. Figure 2 shows this schematically.

After that, the deposition step is repeated to begin the cycle again. The directionality of the etch is controlled by the ion bombardment in its role of aiding the removal of the surface polymer. The polymeric layer has to be deposited with good

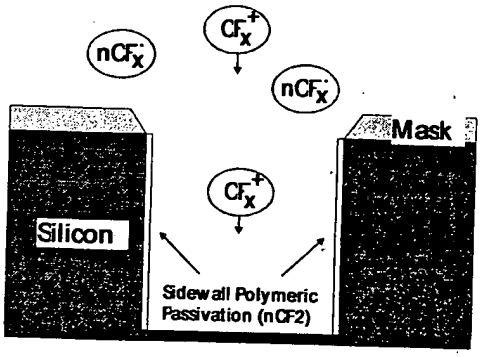

Figure 1: ASE process deposition step

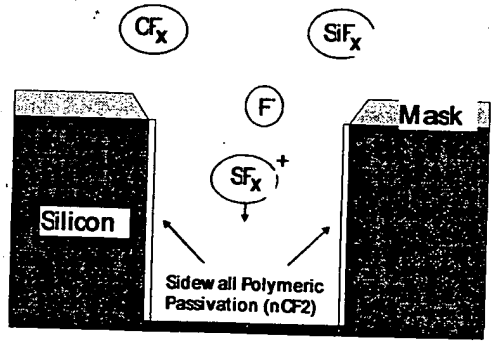

Figure 2 : ASE process etch step

conformity to the given topography and also readily removed by the etching plasma. To control this balance between the etching and the deposition step a careful selection of the used chemistry is required.

The polymeric film used in the ASE process meets these needs, since only low levels of surface ion bombardment in the presence of reactive chemicals are necessary to remove the layer completely from the surface. A suitable etch precursor gas for this technique is SF_6 as used in this ASE process.

Polymeric deposition precursors can be choosen from a range of fluorocarbon chemistries such as CHF_3, C_2F_6 and other higher molecular weight gases. Details of the plasma source technology , the ASE process and the STS ICP have already been presented elsewhere [2].

2.2 Etch equipment

The equipment for the ASE process installed at the Fraunhofer Institute IFT is a STS cluster tool. This model consists of an ICP reactor for the ASE process, a RIE chamber for standard dry etch processes of SiO_2, Si_3N_4 and SiC, a dealer chamber, and a load lock with a cassette system.

The ICP source produces high plasma densities at low pressure. A schematic of the STS ICP reactor (Inductively Coupled Plasma) is shown in figure 3. The ICP as well as the RIE chamber is equipped with mechanical wafer clamping and helium backside cooling to control the temperature of the wafer. The chemistry of the process adopted for the ASE process in the STS-ICP system is nontoxic and non corrosive and the wafer temperature is held close to the ambient.

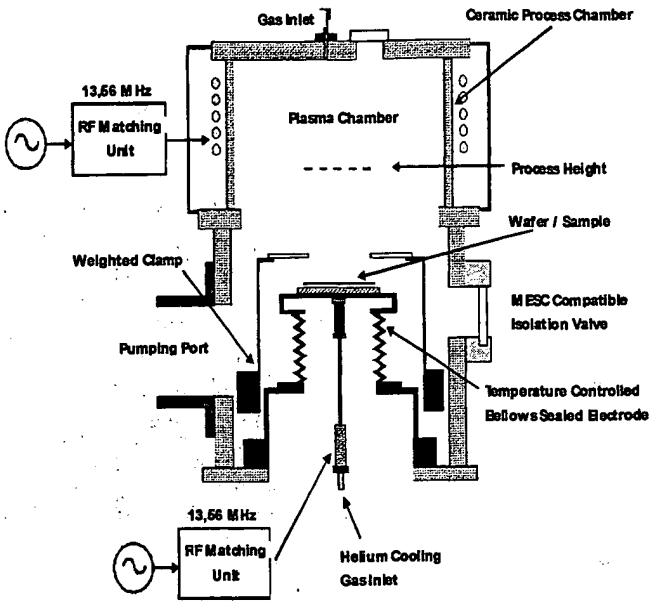

Figure 3: Schematic of STS ICP system

2.3 Etch rates for silicon and passivation materials

The capability of this process is best illustrated by considering a number of MEMS applications fabricated at the Institute. The typical performance of this process is summarized in table 1 and illustrated through the micrographs in figures 5 to 15.

Etch Rate	1.5 to 3.0 µm/min	Etch Depth Capability	2 to 100 µm
Selectivity to Resist	50 to 100:1	Uniformity wafer	± 2.5 to 5%
Selectivity to SiO_2	120 to 200:1	Feature size	1 to > 500 µm
Aspect Ratio	up to 30	Sidewall Profile	89 ± 1°

Table1: Selected data of the present used STS ASE process

2.4 Interdependence between etch rate and geometrical openings

One field of investigation during test and evaluation of the ASE process was the interdependence (figure 4) between the given geometry of the mask layer and the resulting etch depths. Figure 5 shows a typical etch rate behaviour of different structure widths which are closely together. Of course this is not a special ASE problem but the differences have to be taken into account during design, development for and processing a certain device.

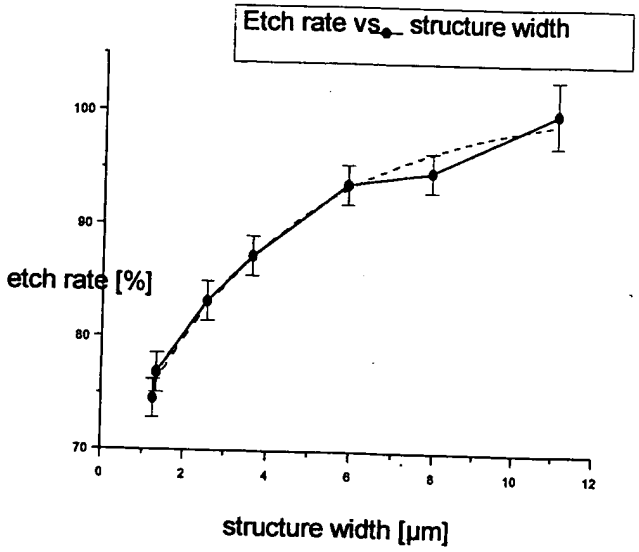

Figure 4: Etchrate versus pattern width

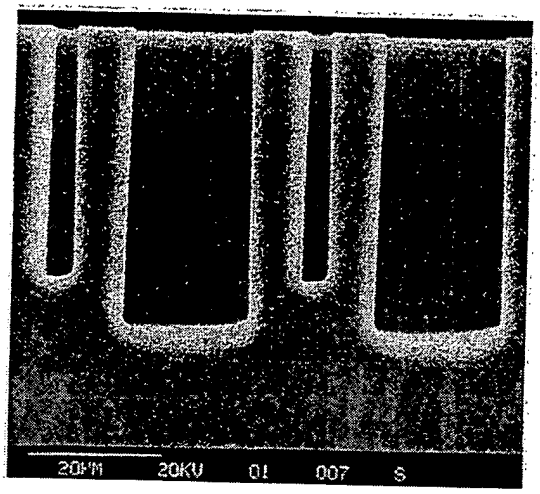

Figure 5: SEM view of etchrate behaviour vs. geometry

3. APPLICATIONS

The combination of bulk-micromachining and ASE etch process for microstructuring of a membrane leads to different possibilities of device structures. Examples are accelerometers or microfluidic components. As already explained in the introduction, only square or rectangle geometrical shapes are generally etched in bulk-micromachining thus leaving the field of polygonal, elliptical or arbitrary shapes to ASE and related techniques.

Wet etchants are used to etch cavities for membrane definition, and the dry etching is used for the critical crystal orientation independent etch steps such as defining sensor beam structures etc.[3] Figure 6 shows a silicon paddle on back etched membrane cavities.

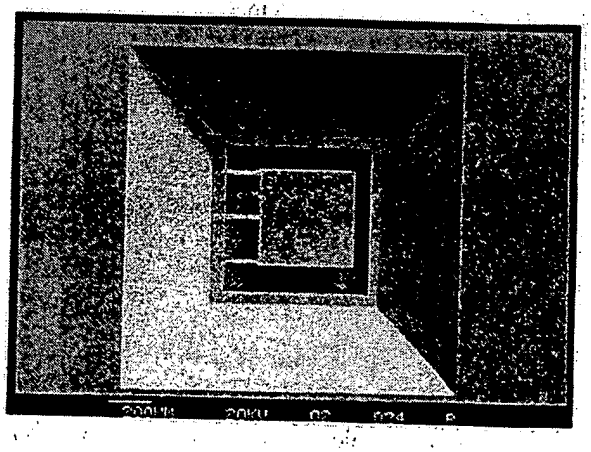

Figure 6: Micrograph of a paddle- membrane test structure

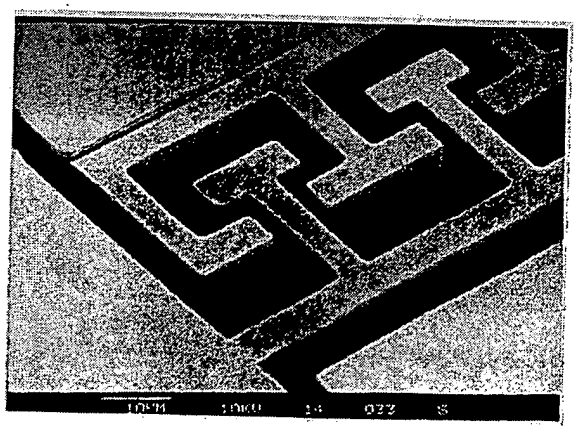

Figure 7: Parts of the microswitch

3.1 Micro switch

Microrelays are one of the most promising future micromachined devices due to a growing need for high speed switching relays e.g. in automatic test equipment or communication devices. Because of fabrication simplicity and low power consumption electrostatic actuation is preferrable. There are two possibilities for the motion of a cantilever beam: A vertical and a lateral switch [4]. The flat capacitor is an often used configuration for electrostatic actuators. The generated forces depend among others on the area of the plate. For microrelay application it is crucial to achieve large forces which cause large contact pressures. Therefore relatively large plates are necessary to get a reasonable relay design. With a deep silicon etching process (ASE) it is possible to structure(figure 7) high aspect ratio beams or plates normal to the wafer plane. Fig.8 shows a 30μm deep cantilever beam and the fixed electrode on the opposite side.

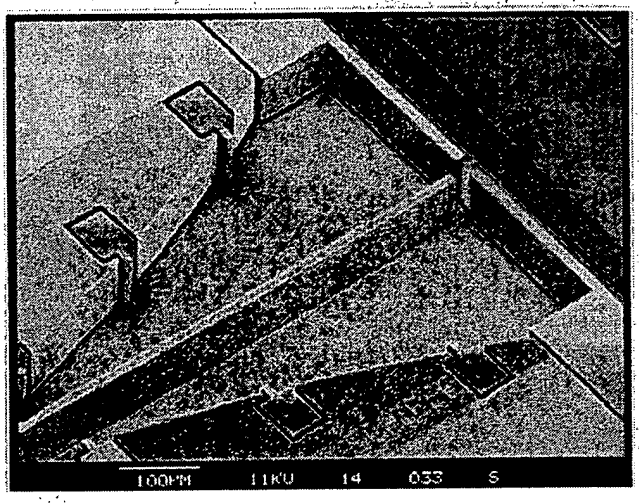

Figure 8: ASE released cantilever beam

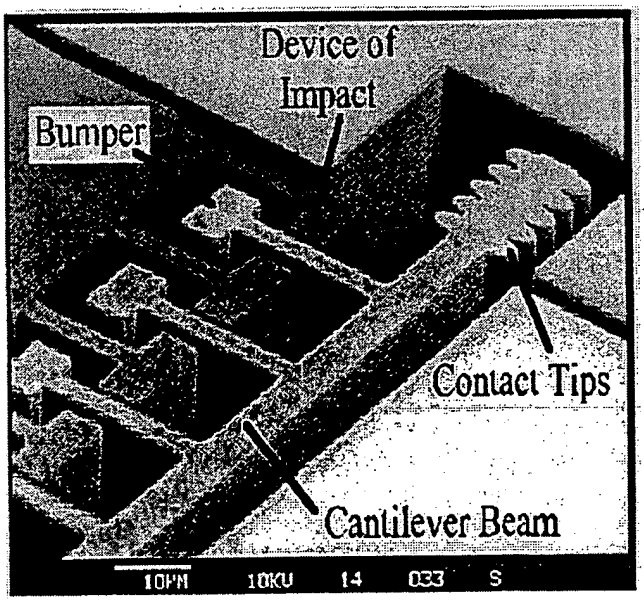

Figure 9: Lateral microrelay

Contact tips are structured on the free end of the beam. They increase the contact pressure which is advantageous to provide a mechanical abrasion of surface films and therefore achieve a low contact resistance with low contact noise. The shape of the contacts can be freely designed.
To prevent short circuiting a physical contact of the actuating electrodes must be avoided. In Fig.8 bumpers are used to hold the cantilever beam back. In the closed state the bumpers come in contact with the device of impact and a further deflection of the cantilever electrode is prevented.
A bounce free operation of the electrostatic lateral microrelay is observed with a switching time of about 30µs. [4]

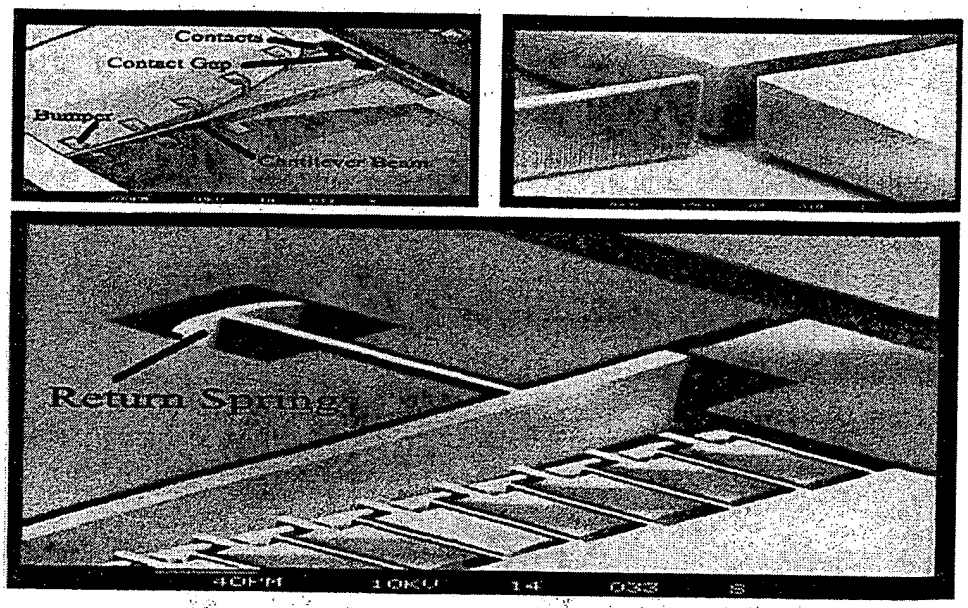

Figure 10: Lateral microrelay with a large contact gap and detail of the beam tip, microrelay design with return spring

The lateral motion switches are fabricated by surface micromachining with a deep silicon etching (ASE) process. The combination with SOI-wafers (silicon on insulator) as the substrate material makes a simple fabrication process possible which only affords two mask layers.
First an adhesion layer (TiW) and gold (Au) is sputtered. Next the metallisation layers are structured to form contact pads and strip conductors. The deep silicon etching process patterns the cantilever beam, the bumpers and the contacts. After time limited etching of the sacrificial SiO_2-layer only the beams are released whereas the other structures are still attached to the substrate. The high stiffness of the beams allows this wet etching without a sticking of the beams after the drying period.

3.2 Microfluidic components

Microchannels are vital parts of our recently introduced integrated microanalytical (VIMAS) and drug-delivery (MEDOS) systems. One of the goals was the miniaturization and standardisation of these modular built devices.

An excellent anisotropic profile, a high aspect ratio and freedom of design and mask layout has allowed a wide range of useful geometries for microfluidic components.like the one shown in figures 11 and 12. A pyrex wafer is bonded to the microchannel array to protect it during handling (figure 13). Since the ASE process uses standard photoresist as an etch mask it is possible to get a simple and cost reducing process flow for volume production.

It was shown that microchannels can be applied for precise flow control [5] which in practice is mainly limited by technological problems concerning the fabrication of very narrow channels. Therefore the development of a new fabrication process using an optimized ASE will be started as a next step.

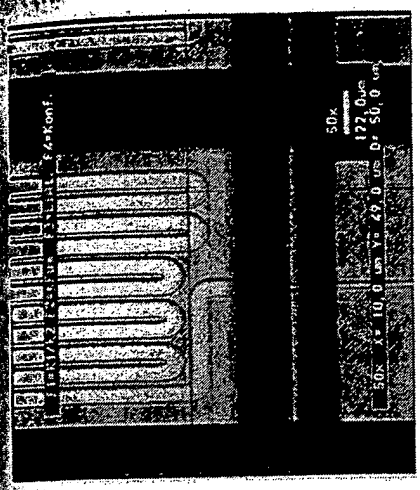

Figure 11: VIMAS microchannel channel

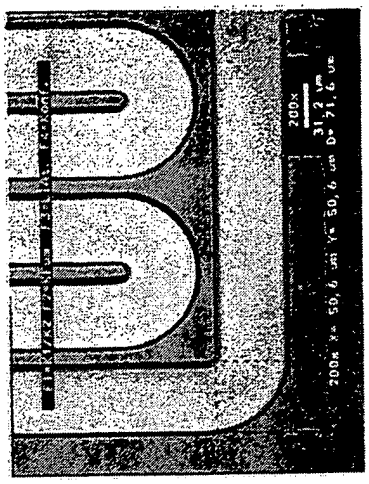

Figure 12: Detailed view from fig. 8

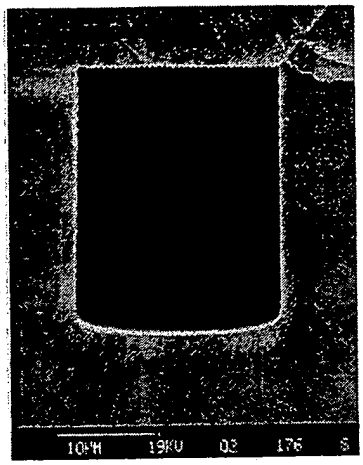

Figure 13: cross section of pyrex-silicon

In the future dosing and flow-control systems can be envisaged which combine micro-fluid channels, pressure and temperature sensors and data aquisition fabricated with the help of an ASE system.

3.3 Silicon micromachined sensors

SOI based capacitance sensors as accelerometers and angular rate sensors are more and more of interest in automotive applications like safety systems. Fabricating methods are under development to cope with the new challenges in this field. Doing this anisotropy is the most critical parameter to be controlled during the etching of close proximity high aspect ratio structures such as these sensors. After etching the sensor structures, they need to be 'released' by removing the under - laying oxide film. Figure 14 shows plates with a gap of 2µm and an etch depth of 30 µm. The etch process stops at the buried oxide of the device wafer. In Figure 15 the essential parts of the device structure can be seen.

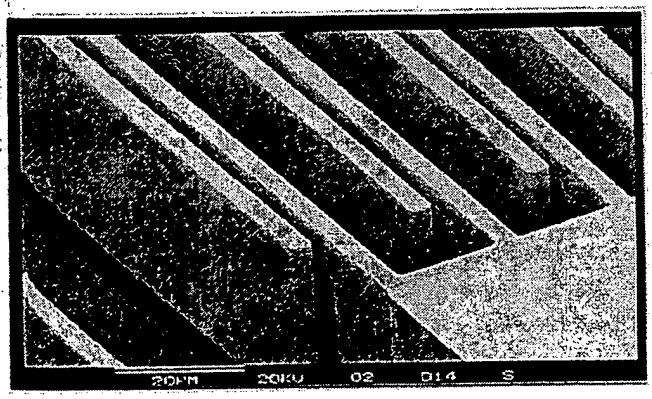

Figure 14: Micrograph of silicon plates with a gap of 2µm.(detail from figure 15)

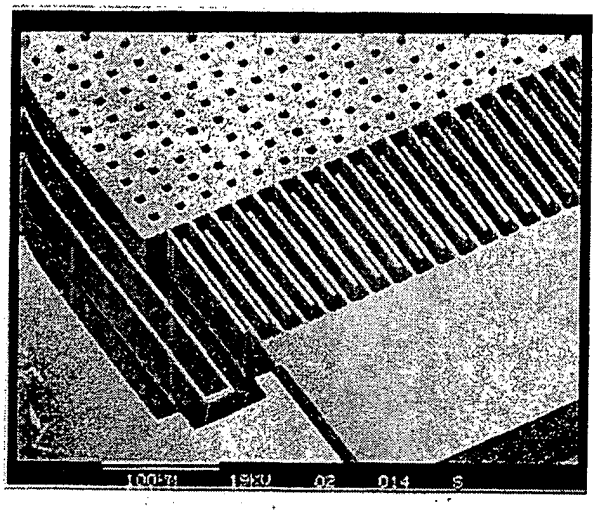

Figure 15: Test structure for displacement sensors

3.4 Vias and Through Wafer Via Holes

Vias between chip layers in vertically integrated circuits (VIC) and through holes for embedded interconnects [6] or as an fluid channel are another application using the ASE process. To etch via holes through a pre-processed wafer for interconnections with another device layer(e.g. sensing elements) needs high etch rates to reduce processing time and costs. But there is always a profile/etch rate trade off which means one has to compromise due to anisotropy. The principle leading to a vertical integration of microelectronic circuits[7] is shown in figure 16. This CMOS compatible interchip via (ICV) concept allows the formation of multiple wafer stacks.

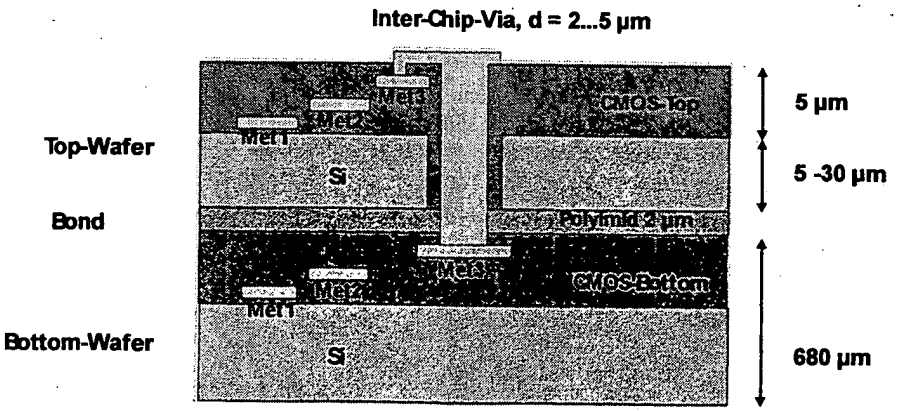

Figure 16: Principle of a vertical integrated circuit

4. CONCLUSIONS

Serveral MEMS projects realized with the assistance of the ASE etch process have been described .We pointed out the design freedom allowed by this new etch tool for the fabrication of the introduced microcomponents and decives. At present, efforts are directed towards optimization of the discussed process. In conclusion, it remains to be stated that the use of the ASE process is attractive for a large variety of applications and an important extension of existing microfabrication technologies.

5. ACKNOWLEDGEMENTS

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Further author information-
K.K.(correspondence): Email: kuehl@ift.fhg.de ; Phone: +49 (0)89 54759 237 ; Fax: +49 (0)89 54759 100 ; WWW: http://www.ift.fhg.de

PATENT

Attorney Docket No.: 0000265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Carley	)	
		)	**Examiner**: Erik Kielin
Serial No.:	09/583,386	)	
		)	**Art Unit**: 2813
Filing Date:	May 30, 2000	)	

Entitled: MANUFACTURING OF MEMS STRUCTURE IN SEALED CAVITY USING DRY-RELEASE MEMS DEVICE ENCAPSULATION

AFFIDAVIT OF DR. L. RICHARD CARLEY

I, Dr. L. Richard Carley, an individual residing at Glen Mitchell Road, Sewickley, Allegheny County, PA, 15143, in the above-referenced application, do hereby declare:

1. I currently hold three degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, S.B. (1976), S.M. (1978) and Ph.D. (1984).

2. I have been a Professor in the Electrical and Computer Engineering Department of Carnegie Mellon University in Pittsburgh, PA since 1984. A portion of my research activities during my tenure at Carnegie Mellon University has involved the design of microelectromechanical systems (MEMS).

3. I currently hold two U.S. Patents in the area of MEMS, U.S. Patent 5,757,631, entitled "Microelectromechanical Structure and Process of Making Same", issued 2/10/98, and U.S. Patent 5,970,315, bearing the same title, issued 10/19/99. Additionally, I currently have three U.S. Patent applications pending before the U.S. Patent and Trademark Office in the area of MEMS.

4. Since 1996, I have authored or co-authored 24 published technical papers in the area of MEMS. A list of these publications is attached hereto.

5. Since 1996 I have been a Principal Investigator or co-Principal Investigator on five major MEMS-related projects.

6. I am currently the founder, Chief Executive Officer and Chief Technology Officer of IC Mechanics, Inc. of 425 N. Craig Street, Suite 500, Pittsburgh, PA 15213, a MEMS company dedicated to the commercial design and production of MEMS devices for a wide variety of applications.

7. I offer these credentials for the purpose of establishing myself as an expert in the field of MEMS qualified to provide testimony on the state of the art and practice in the MEMS field at the time of the filing of the current application on May 30, 2000.

8. At the time of the invention, it was well recognized that the etching of long tunnel-like structures having a small opening to etch distance ratio (aspect ratio) were subject to extremely long etch times, and that, in fact, etch time increased faster than linearly with the length of the tunnel to be etched.

9. It was generally thought that the reason for the long etch times was related to the problem of removing etch by-products from the long tunnels through small openings, and replacing the etch by-products with fresh etchant.

10. For this reason, it was generally believed that the undercutting of large areas under a MEMS device, in an encapsulated environment, could only be economically accomplished with a wet etchant, which generally have much higher concentrations of etching species than dry echants.

11. At the time of the invention, I was unaware of anyone using oxygen plasma, introduced through small holes, to undercut large areas of sacrificial material to release an encapsulated MEMS device from its substrate.

12. At the time of the invention, I was also unaware of anyone using a barrel etcher to release encapsulated MEMS devices.

13. Because of the aforementioned long etch times, it was generally thought at the time of the invention that the release of an encapsulated MEMS devise using a non-liquid

etchant was commercially infeasible.

14. At the time of the invention I was unaware of anyone using a non-liquid etchant, and, in particular, oxygen plasma, to release encapsulated MEMS devices.

Dr. L. Richard Carley, Ph.D.

9/18/02
Date

2 Patents issued in MEMS process area:

CMU sponsored patent application: "Microelectromechanical structure and process of making same," Inventors: L. R. Carley, M. L. Reed, G. K. Fedder, and S. Santhanam. Application filed 25 July 1995. U.S. Patent No. 5,757,631 issued February 10, 1998.

CMU sponsored patent application: "Microelectromechanical structure and process of making same," Inventors: L. R. Carley, M. L. Reed, G. K. Fedder, and S. Santhanam. Continuation in Part of (7), Application filed 3 October 1997. U.S. Patent No. 5,970,315 issued October 19, 1999.

24 Papers in MEMS area published in refereed Journals and Conference Proceedings:

G. K. Fedder, S. Santhanam, M. L. Reed, S. C. Eagle, D. F. Guillou, M. S.-C. Lu, and L. R. Carley, "Laminated High-Aspect-Ratio Microstructures in a Conventional CMOS Process", Proceedings of the 9th IEEE International Workshop on Micro Electro Mechanical Systems, San Diego, CA USA, Feb. 11-15, 1996.

L. Richard Carley, David F. Guillou, and Suresh Santhanam, "Fabrication and Performance of Mesa Interconnect," Proceedings of the International Symposium on Low Power Electronic Systems, Monterey CA, August 1996.

G. K. Fedder, S. Santhanam, M. L. Reed, S. C. Eagle, D. F. Guillou, M. S.-C. Lu, and L. R. Carley, "Laminated High-Aspect-Ratio Microstructures in a Conventional CMOS Process", Sensors & Actuators A, vol. A57, no. 2, pp. 103-110, November 1996.

L. R. Carley, D. Guillou, and G. Fedder, "Design of a MEMS Actuated Scanning Probed-Based Data Storage System," Proceedings of the 1997 IDEMA Alternative Storage Technologies Symposium, San Jose, CA, June 1997.

M. S.-C. Lu, S. Santhanam, L. R. Carley, and G. K. Fedder, "Curved-Electrode Lateral Electrostatic Microactuators in 0.5μ CMOS," Proceedings of the 9th Int. Conf. on Solid-State Sensors and Actuators (Transducers'97), Chicago IL, June 1997.

D. F. Guillou, S. Santhanam, and L. R. Carley, "Laminated, sacrificial-poly MEMS technology in standard CMOS," Proc. Eurosensors XIII, pp. 339-340, The Hague, The Netherlands, Sept. 1999.

L. R. Carley, J.A. Bain, G.K. Fedder, D.W. Greve, D.F. Guillou, M.S.-C. Lu, T. Mukherjee, S. Santhanam, L. Abelmann and S. Min, "Single-chip computer with MEMS-based magnetic memory," Proc. 44th Annual Conf. on Magnetism and Magnetic Materials (MMM '99), San Jose, CA, Nov. 1999.

L. R. Carley, J. A. Bain, G. K. Fedder, D. W. Greve, D. F. Guillou, M. S. C. Lu, T. Mukherjee, S. Santhanam, L. Abelmann, and S. Min, "Single Chip Computers With MEMS-Based Magnetic Memory," Journal of Applied Physics, vol. 87, no. 9, pp. 6680-6685, 1 May 2000.

D. F. Guillou, S. Santhanam, and L. R. Carley, "Laminated, Sacrificial-Poly MEMS Technology in Standard CMOS," Sensors and Actuators A, vol. A85, no.1-3, p. 346-55, 25 Aug. 2000.

L. R. Carley, G. R. Ganger, and D. F. Nagle, "MEMS-based integrated-circuit mass-storage systems," Communications of the ACM, vol.43, no.11, p. 72-80, Nov. 2000.

Q. Jing, H. Luo, T. Mukherjee, L. R. Carley, G. K. Fedder, "A 1 mG lateral CMOS-MEMS accelerometer," Proceedings IEEE Thirteenth Annual International Conference on Micro Electro Mechanical Systems, pp. 187-92, Miyazaki, Japan; 23-27 Jan. 2000.

H. Luo, G. K. Fedder, and L. R. Carley, "CMOS micromechanical bandpass filter design using a hierarchical MEMS circuit library," Proceedings IEEE Thirteenth Annual International Conference on Micro Electro Mechanical Systems, pp. 502-07, Miyazaki, Japan; 23-27 Jan. 2000.

L. R. Carley, Greg Ganger, David Guillou, and David Nagle, "System Design Considerations for MEMS-Actuated Magnetic Probe Based Mass Storage", Digests of The Magnetic Recording Conference (TMRC'00), pp. B6.1-6, Santa Clara CA, 14-16 Aug. 2000.

J.-F. Wu and L. R. Carley, "Table-Based Time-Domain Simulation of Oversampled Discrete-Time Microelectromechanical Systems", Proceedings of the IEEE/ACM Int. Workshop on Behavioral Modeling and Simulation (BMAS), Orlando, FL, 2000.

H. Luo, G. K. Fedder, L. R. Carley, "An Elastically Gimbaled Z-Axis CMOS-MEMS Gyroscope," in International Symposium on Smart Structures and Microsystems 2000," Hong Kong, Oct. 19-21, 2000.

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J.-F. Wu and L. R. Carley, "A Simulation Study of Electromechanical Delta-Sigma Modulators", in Proceedings of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS), Sydney, Australia, May 2001.

L. R. Carley, Greg Ganger, David Guillou, and David Nagle, "System Design Considerations for MEMS-Actuated Magnetic Probe Based Mass Storage", IEEE Transactions on Magnetics, vol. 37, no. 2, pp. 657-662, March 2001.

Hasnain Lakdawala, Xu Zhu, Hao Luo, Suresh Santhanam, L. Richard Carley, and Gary K. Fedder, "Micromachined Hi-Q Inductors in a 0.18um Copper Interconnect Low-K Dielectric CMOS Process," in Proceedings of the 2001 Custom Integrated Circuits Conference (CICC'01), pp. 579-582, San Diego, CA, May 2001.

L. Richard Carley, Rany Tawfik El-Sayed, David F. Guillou, Fernando Alfaro, Gary K. Fedder, Stephen Schlosser, David Nagle, Greg Ganger, and James Bain, "MEMS Memory Elements," Keynote Paper in Proceedings of the 2001 Non-Volatile Memory Technology Symposium (NVMTS-01), pp. 1-5, San Diego CA, Nov. 7, 2001.

Jiangfeng Wu, Gary K. Fedder, and L. Richard Carley, "A Low-Noise Low-Offset Chopper Stabilized Capacitive Readout Amplifier," in Digest of Technical Papers of the International Solid-State Circuits Conference (ISSCC), San Francisco, CA, Feb. 6, 2002.

Rany Tawfik El-Sayed and L. Richard Carley, "Performance Analysis of Beyond 100 Gb/in2 MFM-Based MEMS-Actuated Mass Storage Devices," in the Proceedings of the International Conference on Magnetics (INTERMAG), Apr. 2002.

Hasnain Lakdawala, Xu Zhu, Hao Luo, Suresh Santhanam, L. Richard Carley, and Gary K. Fedder, "Micromachined Hi-Q Inductors in a 0.18um Copper Interconnect Low-K Dielectric CMOS Process," accepted for publication in IEEE Journal of Solid State Circuits, in March 2002.

Hao Luo, Gang Zhang, L. Richard Carley and Gary K. Fedder, "A Post-CMOS Micromachined Lateral Accelerometer," accepted for publication in Journal of Microelectromechanics Systems (JMEMS), in April or June, 2002.

In all I have been Principal Investigator or Co-PI on Federal Research Funding: for MEMS research totaling
over $12M over an 8 year period:

Defense Advanced Research Projects Agency (DARPA), "Silicon Micro-Disk Arrays for Data Storage," Principal Investigator, 1 June 1994 – 31 Jan. 1998, $938,403.

Defense Advanced Research Projects Agency (DARPA), "Foundations of Microelectromechanical System Synthesis," Co-Principle Investigator, August 27, 1996 - August 26, 1999, $3,643,788.

Defense Advanced Research Projects Agency (DARPA), "Integrated MEMS Inertial Measurement Unit," Co-Principle Investigator, July 1997 – July 2000, $3,141,721.

Defense Advanced Research Projects Agency (DARPA), "Ultra-High-Density Data Cache for Low-Power Communications," Co-Principle Investigator, September 1, 1998 – August 31, 2001, $3,252,121.

National Aeronautics and Space Administration (NASA), "MEMS-Actuated Magnetic-Probe-Based Mass Data Storage," Principal Investigator, Advanced Cross-Enterprise Technology Development for NASA Missions program, 5/1/01-4/30/04, $1,930,343.